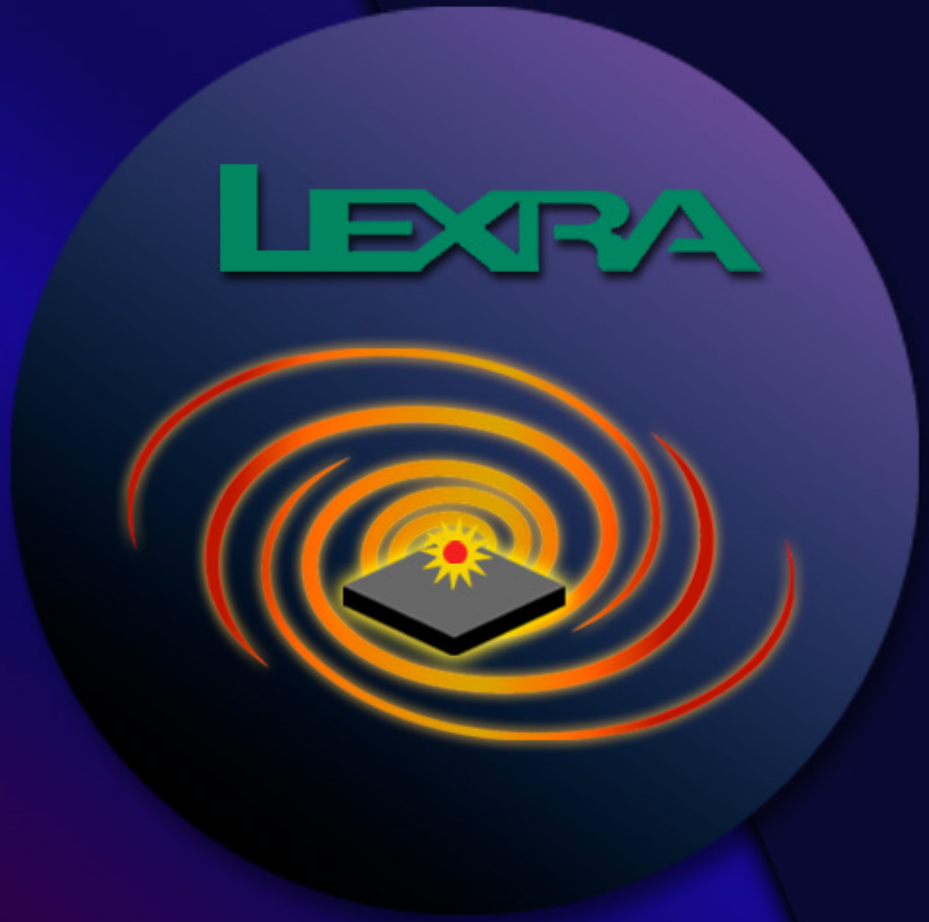


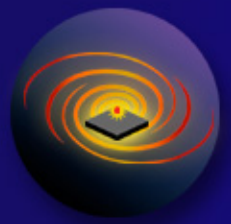
LX5380

RISC-DSP for New Internet Applications

Pat Hays, Chris Hanna,

Jonah Probell

October 25, 2001

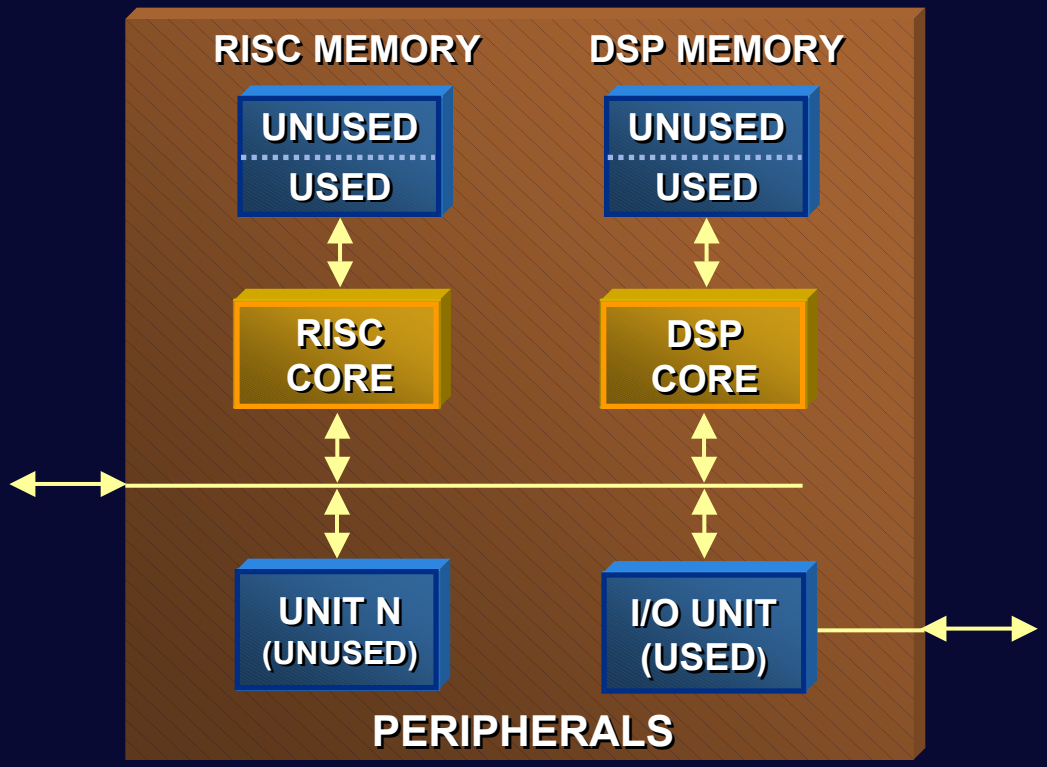


Outline

- Benefits of RISC-DSP Cores
- The LX5380 RISC-DSP
- Example: 3G Wireless Handset
- Example: VoIP Gateway
- Roadmap
- Summary

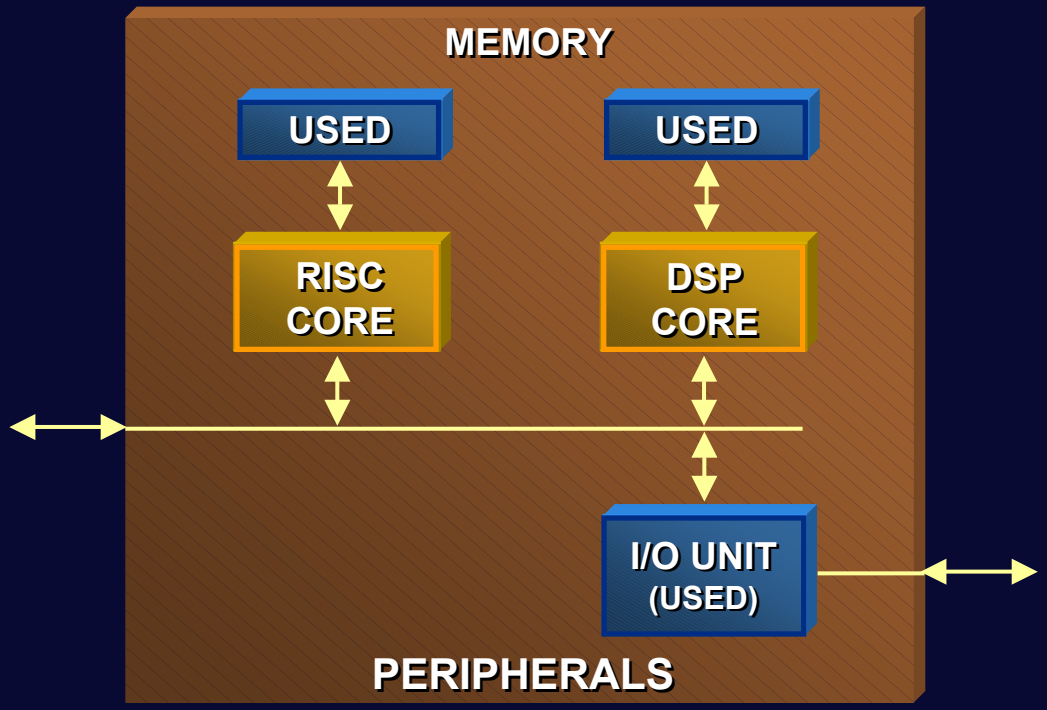
Benefits of RISC-DSP Cores

Cost and Power-Sensitive Designs



Benefits of RISC-DSP Cores

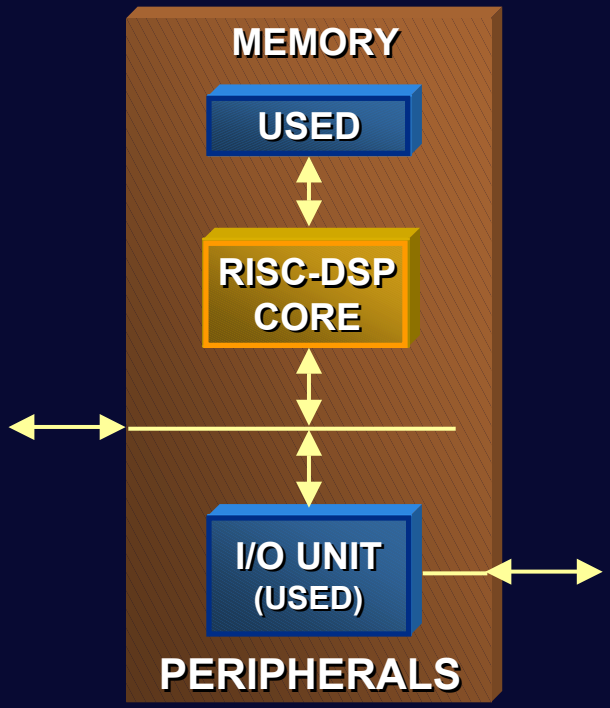
Cost and Power-Sensitive Designs



- Core Benefit → Tailor resources

Benefits of RISC-DSP Cores

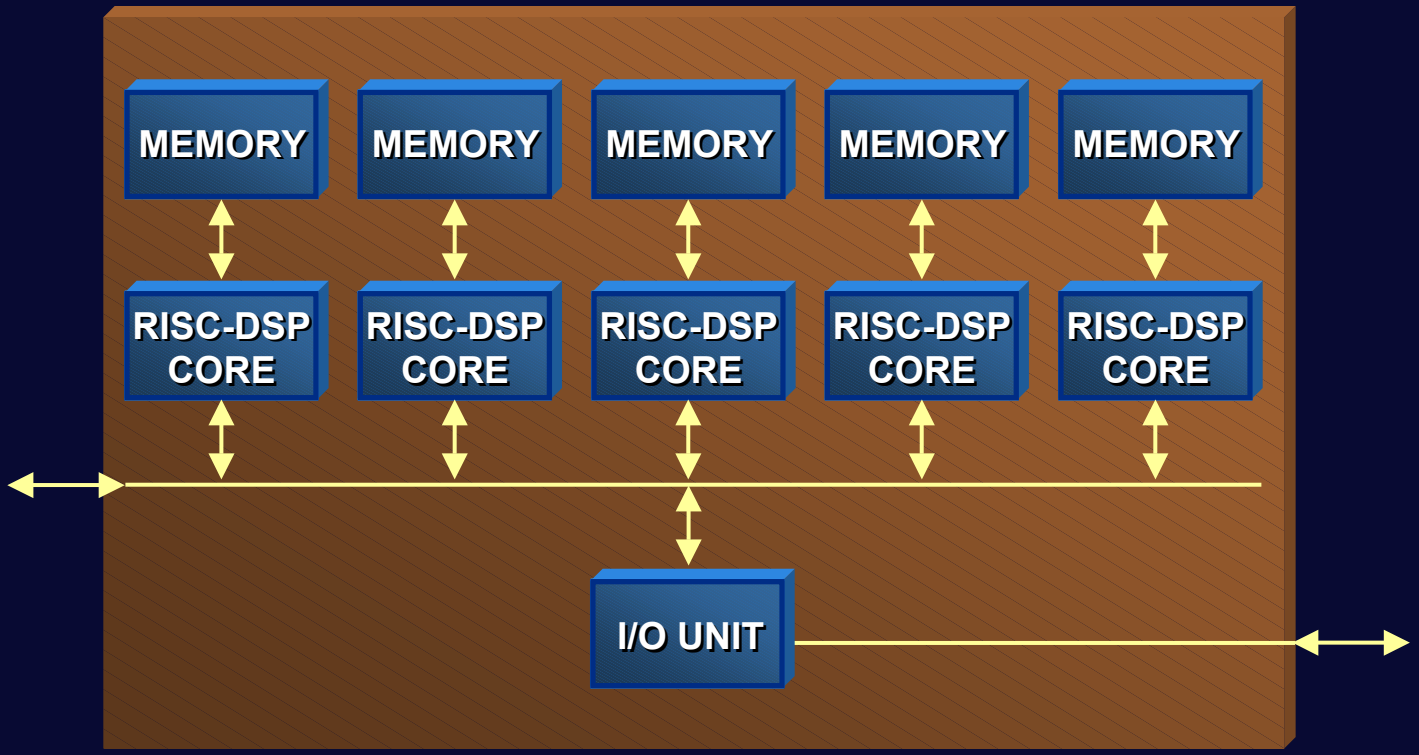
Cost and Power-Sensitive Designs



- Core Benefit → Tailor resources
- RISC-DSP Benefit → Single processor
- New Requirement → Memory Management

Benefits of RISC-DSP Cores

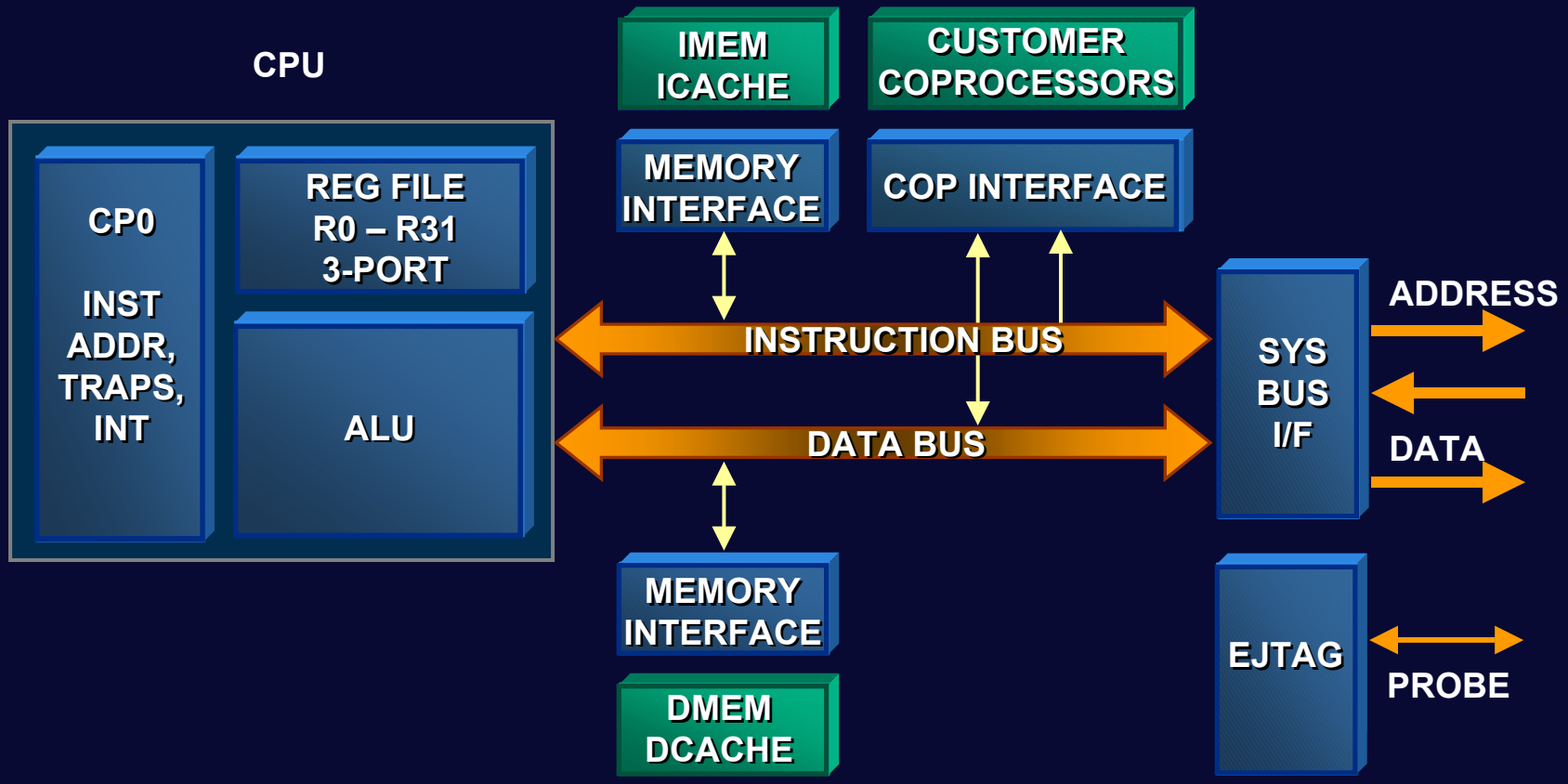
High-Performance, Multi-Channel Designs



- Core Benefit → On-chip Multi-Processing
- RISC-DSP Benefit → Excellent S/W Tools
- New Requirement → Higher Performance

Evolution of the LX5380 RISC-DSP

Start with a 32-bit LX4180 RISC (1998)

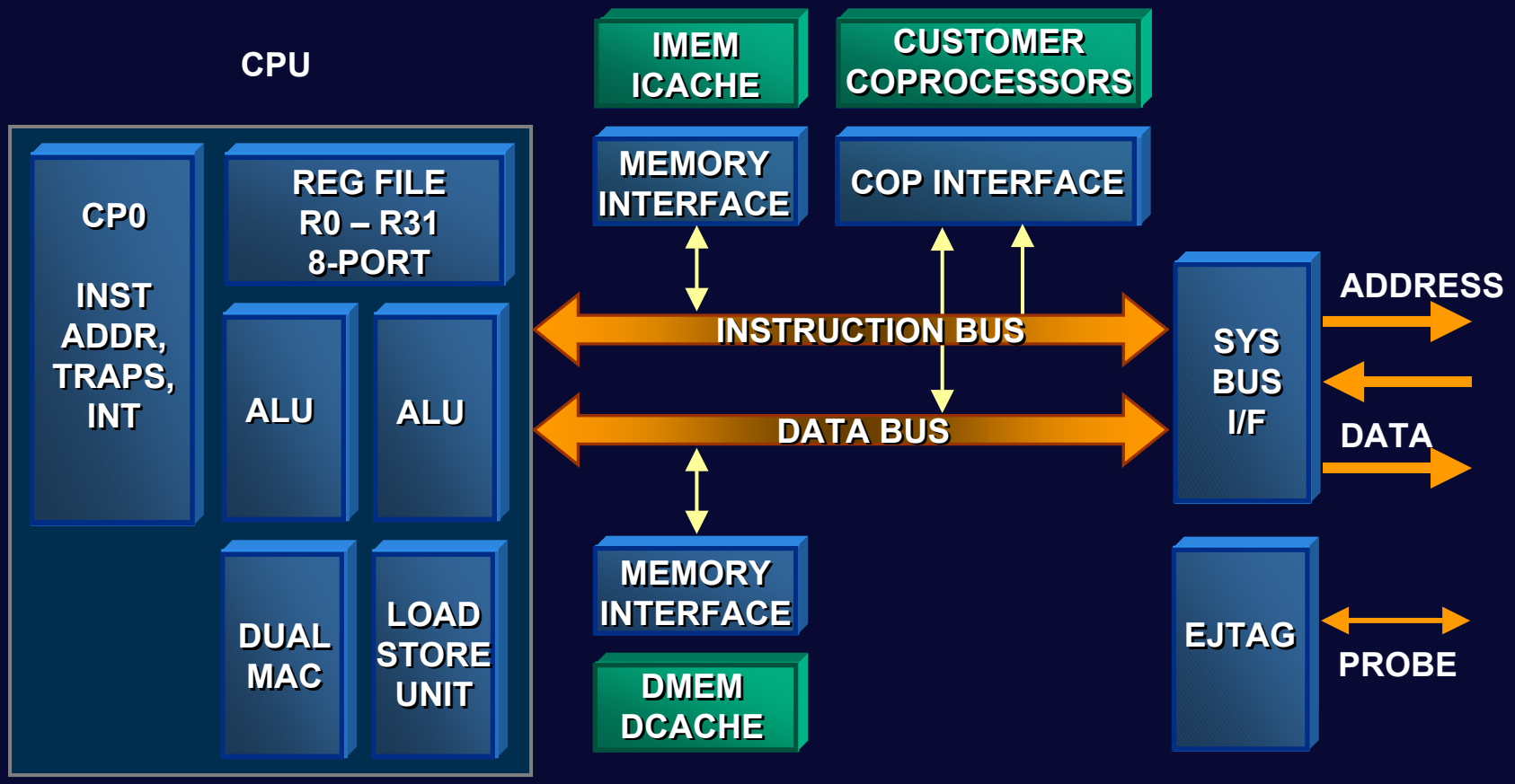


Add a 2nd execution pipeline, dual MAC and DSP instructions…

Provided by Lexra

Evolution of the LX5380 RISC-DSP

LX5280: Superscalar RISC-DSP (1999)

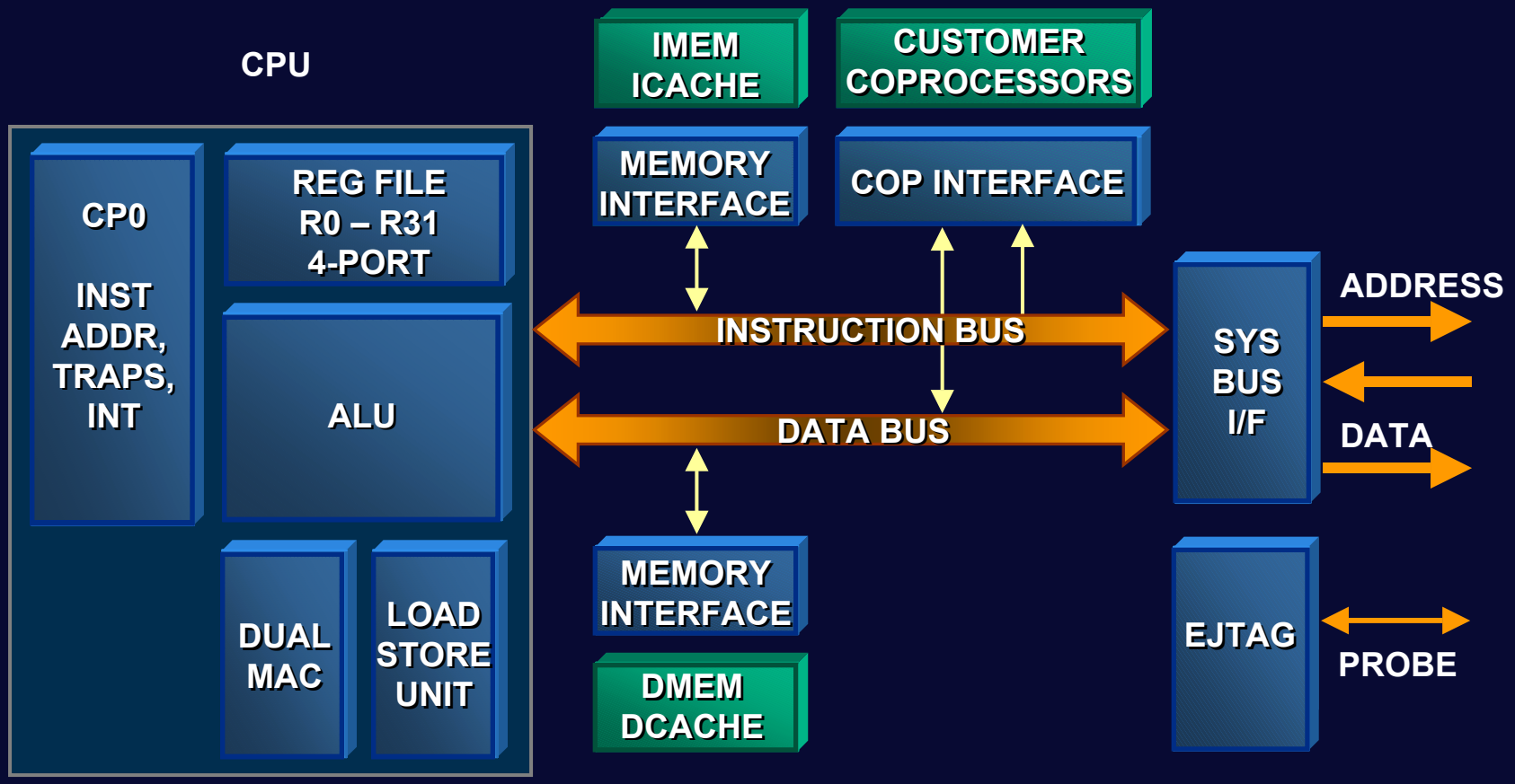


A single pipeline implementation for lower cost, lower power…

Provided by Lexra

Evolution of the LX5380 RISC-DSP

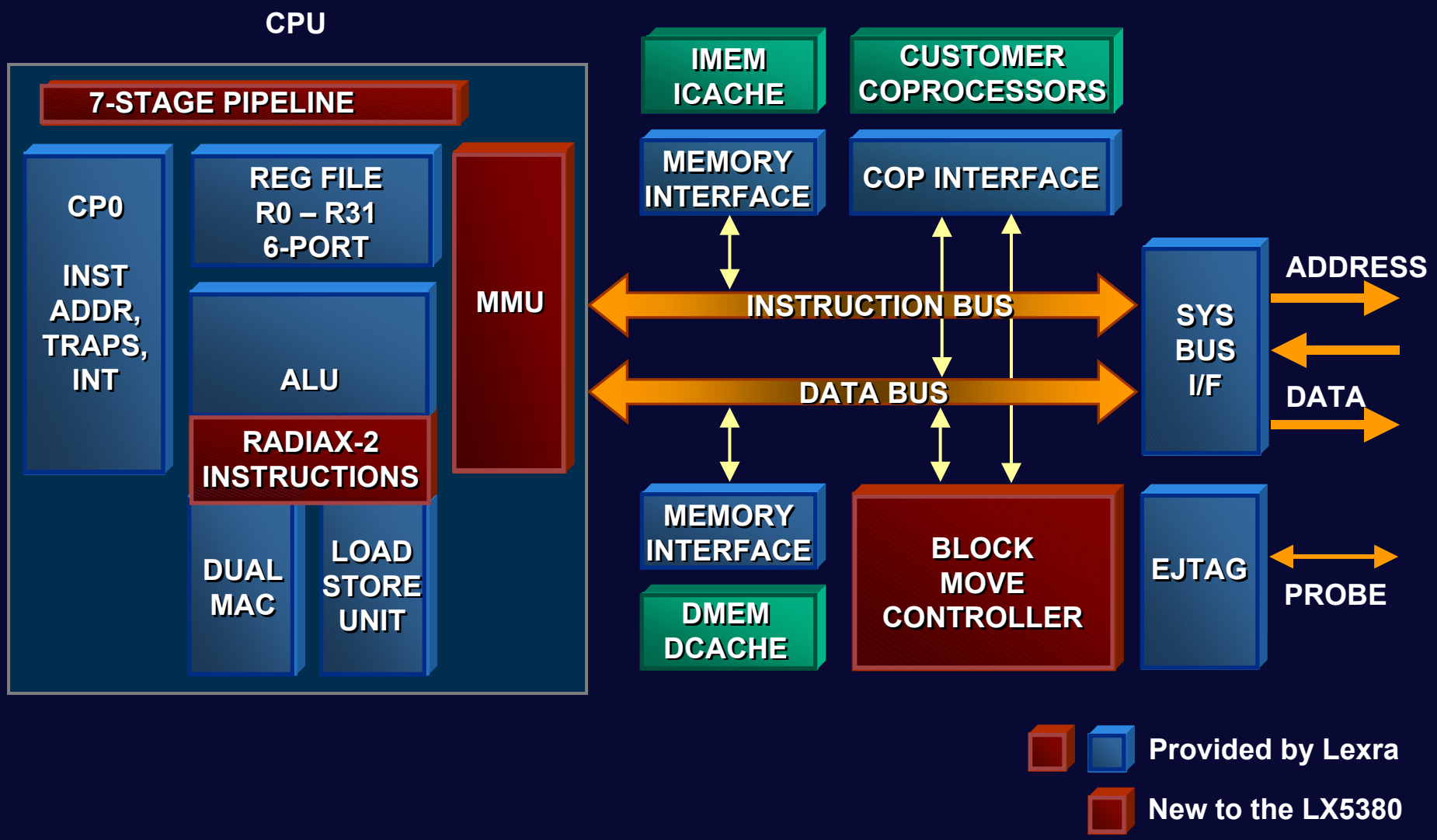
LX5180: Low-cost RISC-DSP (2000)



Add new RISC and new DSP features…

Evolution of the LX5380 RISC-DSP

LX5380 RISC-DSP (2001)

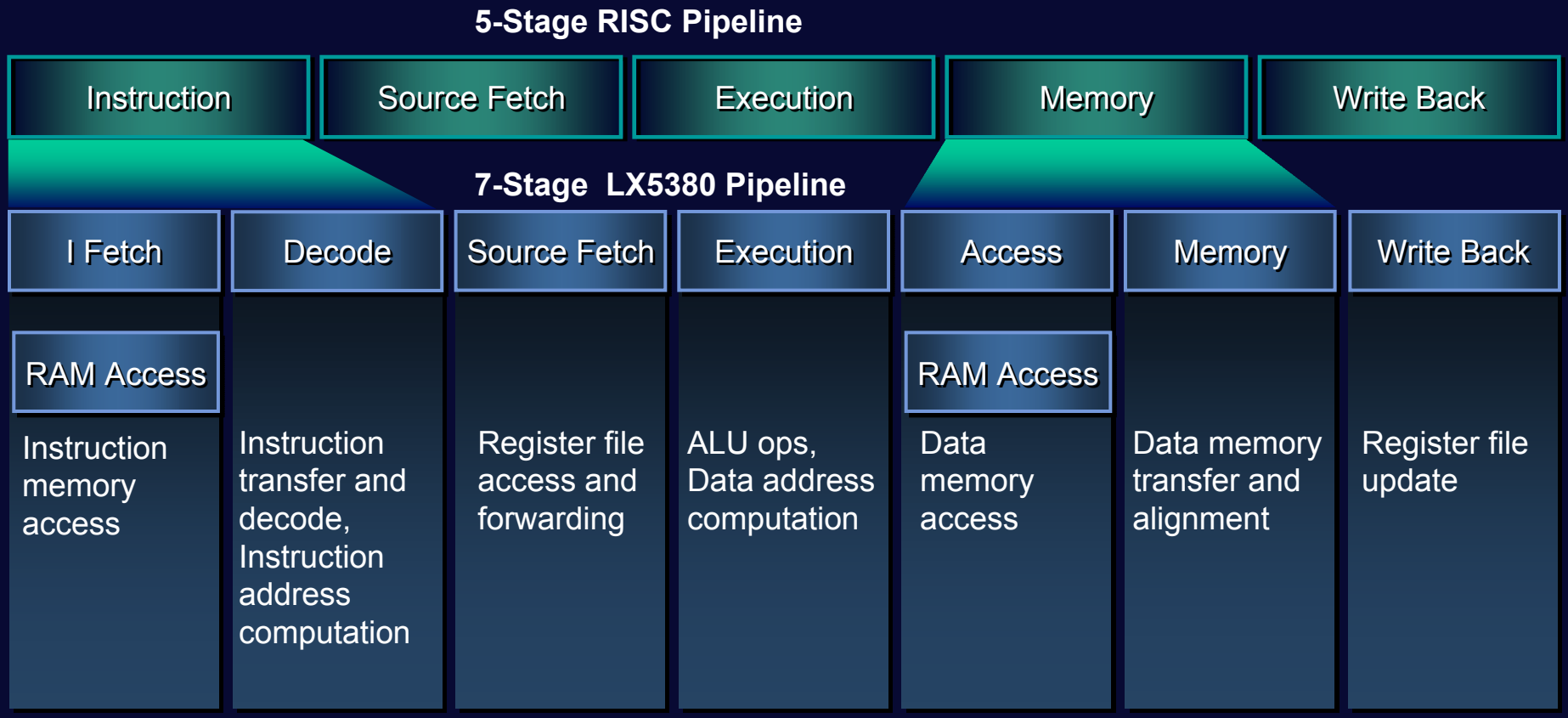


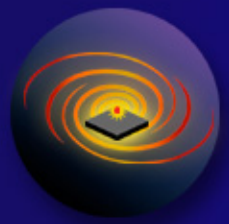
Summary of New LX5380 Features

NEW FEATURE	RISC BENEFIT	DSP BENEFIT
MEMORY MANAGEMENT UNIT	O/S PROTECTION FOR 3RD PARTY CODE	
IMPROVED CACHES (2-WAY SET, WRITE BACK)	REDUCED SYSTEM BUS ACTIVITY	
7-STAGE PIPELINE	FASTER CLOCK	FASTER CLOCK
64-BIT SYSTEM BUS	FASTER DATA TRANSFER	FASTER DATA TRANSFER
BLOCK MOVE CONTROLLER		BACKGROUND TRANSFER OF BUFFERED SAMPLES
20 NEW RADIAX-2 INSTRUCTIONS BIT-FIELD OPERATIONS 32-BIT DSP OPERATIONS PERFORMANCE OPTIMIZATIONS		BETTER 32-BIT ARITHMETIC FOR AUDIO EFFICIENT PACKET PROCESSING IMPROVED COMPILATION

LX5380 7-Stage Pipeline

Positive-edge only. Full-cycle for memory.

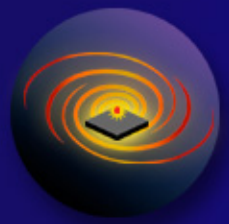




LX5380 Processor

Specifications–Synthesized RTL (0.13 µm LV)

- Performance measures:
  - Clock (wc process, wc conditions) 360 MHz
  - Clock (typ process, wc conditions) 420 MHz
  - Peak 16-bit operations 2 MACs/cycle
  - A(N) • B(N), 32-bit precision 2N cycles
- Power dissipation (wc conditions) 0.2 mW/MHz
- Die area (no memory, MMU, BMC) 1.9 mm^2



Example: 3G Wireless Handset
Requirements

- Ultra low-cost, low-power
  - Hardware for well-defined functions, but…
- Flexible platform for new features
  - Demands programmability
- Open platform
  - Operating systems: EPOC, Windows CE, Linux, OSE, JAVA

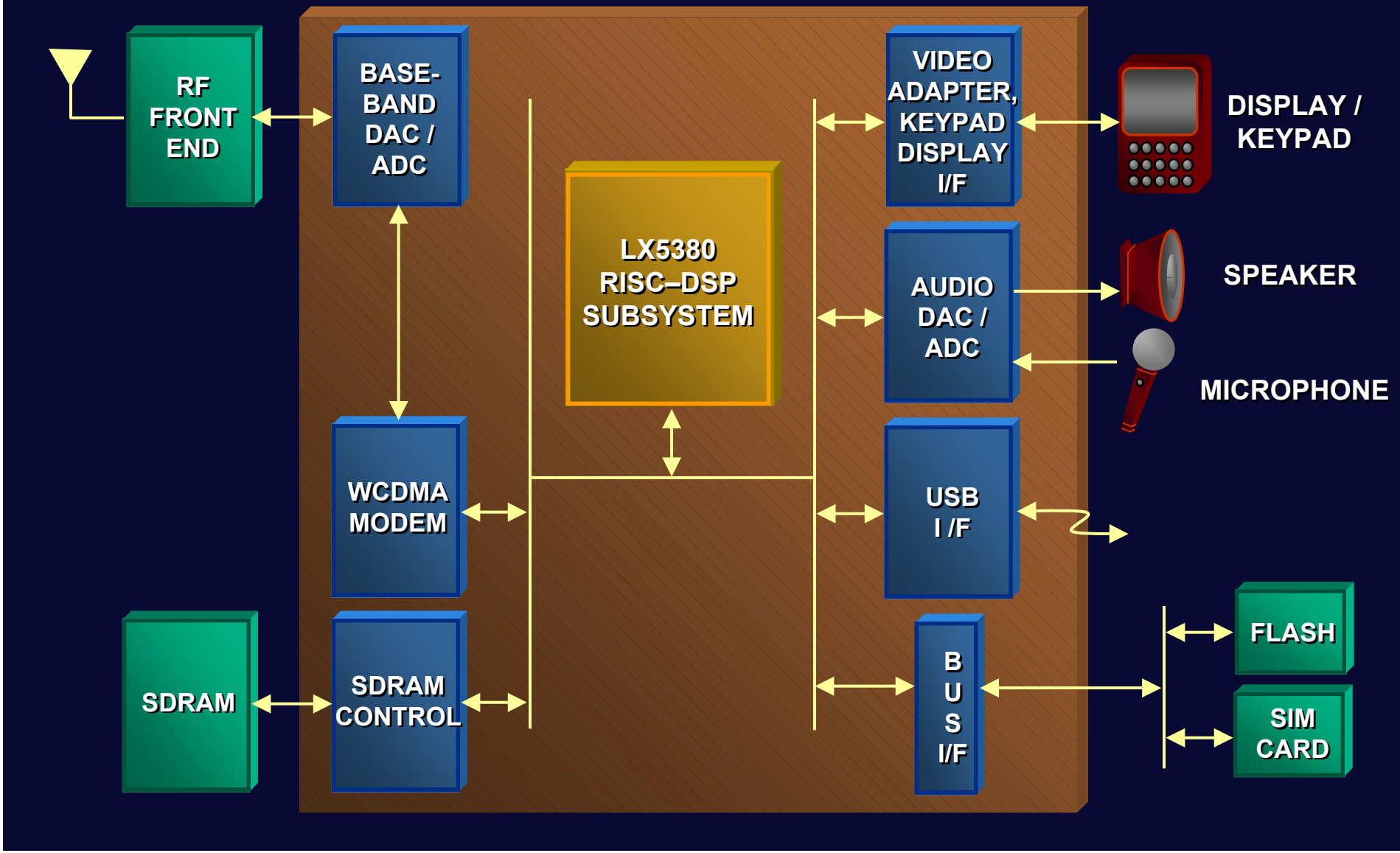
Example: 3G Wireless Handset

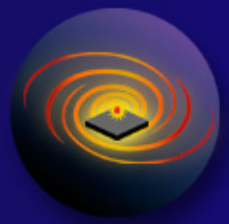
LX5380 Processing Tasks

PROCESSING TASKS	RISC-DSP WORKLOAD
DSP TASKS	
CDMA EVRC SPEECH CODEC	38 MHz
AUTOMATIC GAIN CONTROL AND MIC ARRAY	7 MHz
ACOUSTIC ECHO CANCELLER (32 ms WINDOW)	10 MHz
MP3 DECODE	32 MHz
AUDIO MIXER	2 MHz
MPEG-4 QCIF DECODE (15 FPS)	16 MHz
MPEG-4 QCIF ENCODE (15 FPS)	62 MHz
SPEEECH RECOGNIZER (LIMITED VOCABULARY)	N/A
COMMUNICATIONS PROTOCOLS (384 KBPS)	10 MHz
QVGA RENDERING (15 FPS)	16 MHz
I/O	2 MHz
RTOS AND JAVA VIRTUAL MACHINE	5 MHz
TOTAL	200 MHz

Example: 3G Wireless Handset

Block Diagram of LX5380 Solution





Example: VoIP Gateway
Requirements

- Phone-to-network connectivity
  - Reduce system and customer cost
  - Enable new services. E.g. “follow-me”
- Extensive RISC and DSP program tasks
- Scalability
  - SoHo 4 – 24 channels
  - Enterprise hundreds of channels
  - Central Office thousands channels

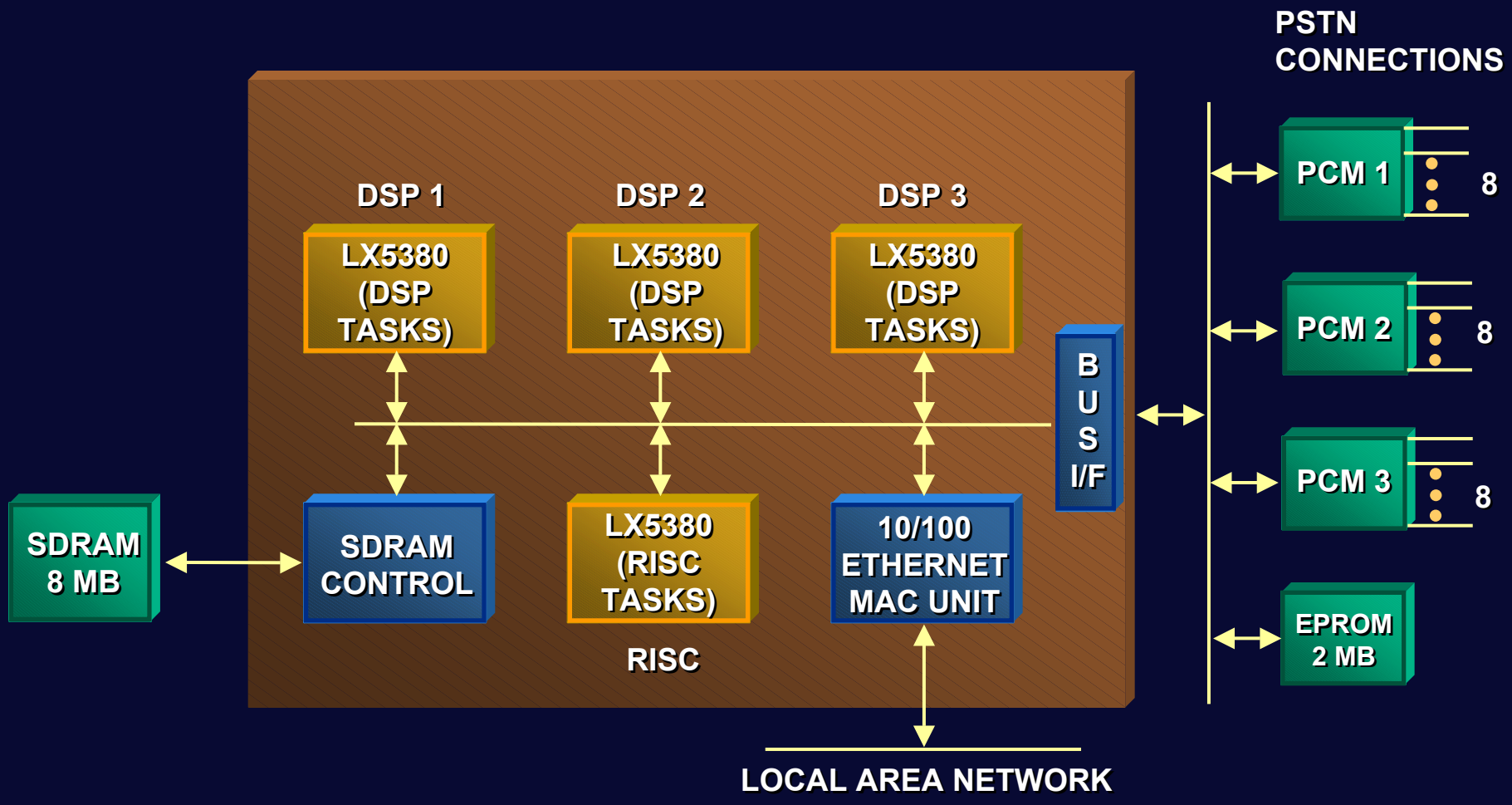
Example: VoIP Gateway

LX5380 Processing Tasks

PROCESSING TASKS	RISC WORKLOAD (24 CHANNELS)	DSP WORKLOAD (8 CHANNELS)
SIGNAL PROCESSING		
CODECS (G.711, G.726, G.723.1, G728, G729A)		156 MHz (WORST CASE)
ECHO CANCELLATION (G.165, G.168, 32ms TAIL)		58 MHz
DTMF DETECT/GEN		18 MHz
VOICE ACTIVITY DETECT (VAD), COMFORT NOISE GEN (CNG), SIGNAL CLASSIFICATION		22 MHz
PACKET PROCESSING		
ENCAPSULATE/ DE-ENCAPSULATE, ADAPTIVE JITTER BUFFER, LOST PACKET COMPENSATION		10 MHz
TELEPHONY SIGNALING/CONTROL		
CALL PROCESSING, ADDRESSING, H.323 PROTOCOLS	26 MHz	
NETWORK PROTOCOL TCP/IP STACK	30 MHz	
NETWORK MANAGEMENT AND APPLICATION LAYER SNMP (MIB) FIREWALL, SIP, HTTP SERVER, USER I/F	100 MHz (AVAILABLE)	
I/O	2 MHz	1 MHz
RTOS	2 MHz	1 MHz
TOTAL	160 MHz	266 MHz

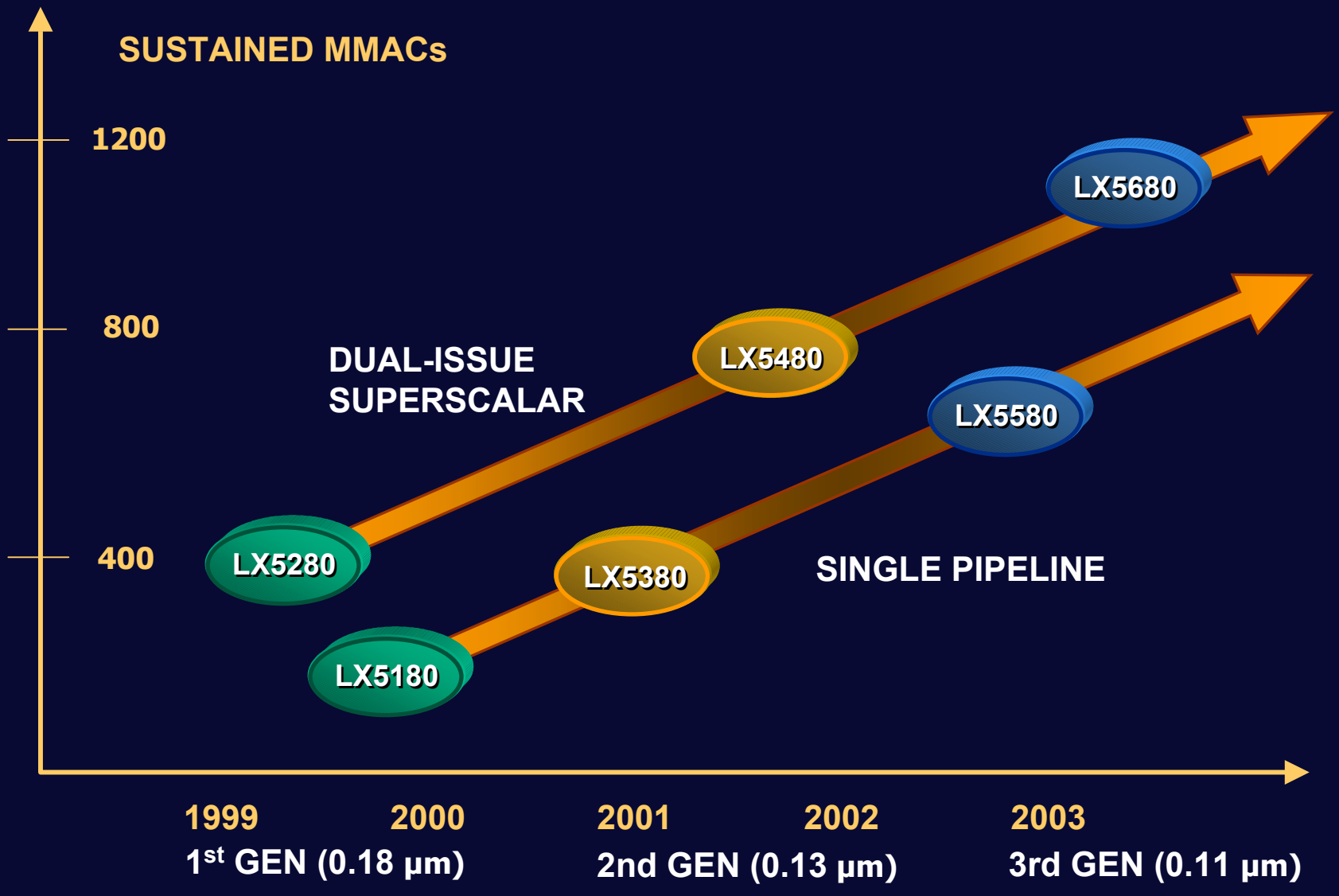
Example: VoIP Gateway

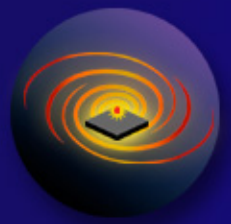
The LX5380 SoHo Solution



24 channels. Scales to support 256 channels

LX5xxx RISC-DSP Roadmap





Summary

- *New internet-enabled applications demand a convergence of RISC and DSP functionality*
- *RISC-DSP cores achieve*
  - *Low cost, low-power in single core applications*
  - *High performance in multi-channel applications*
- *The LX5380 extends both the RISC and DSP benefits of Lexra's RISC-DSP product line*