LX5280

High-Performance RISC-DSP for IP Licensing

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Goal: Licensed RISC-DSP for SoC Designs

- **LOW COST, LOW POWER** in single-processor SoC designs
  - Products: G3 cell phones, ADSL modems
  - Challenge: eliminate redundant subsystems
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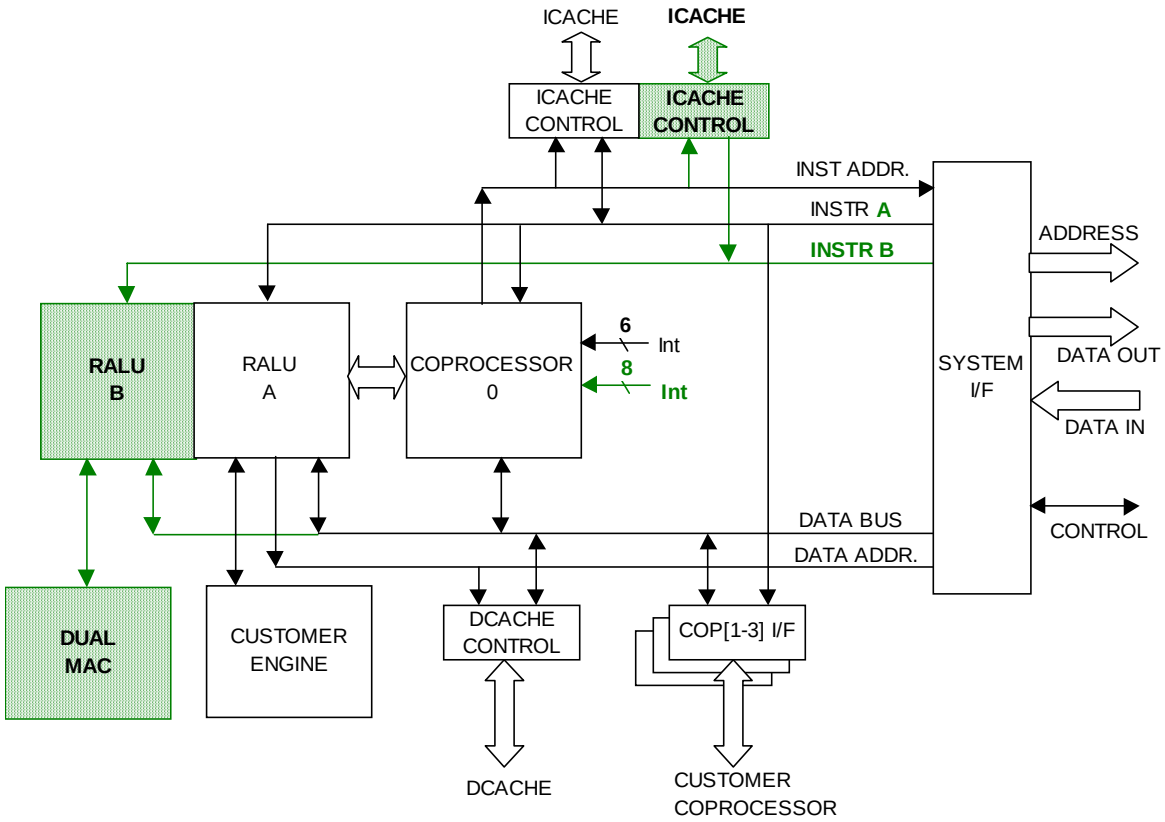
- **HIGH PERFORMANCE** in multi-channel SoC designs
  - Products: wireless basestations, VoIP gateways
  - Challenge: support multi-processor ICs

Outline

- Architecture
- Instruction Set
- Program Development
- Implementation
- Summary

Architecture: Overview



- **A configurable processor subsystem for SoC design**
- **DSP extensions**
  - Superscalar, 7-stage pipeline
  - Low-overhead interrupts
  - New instructions, dual MAC
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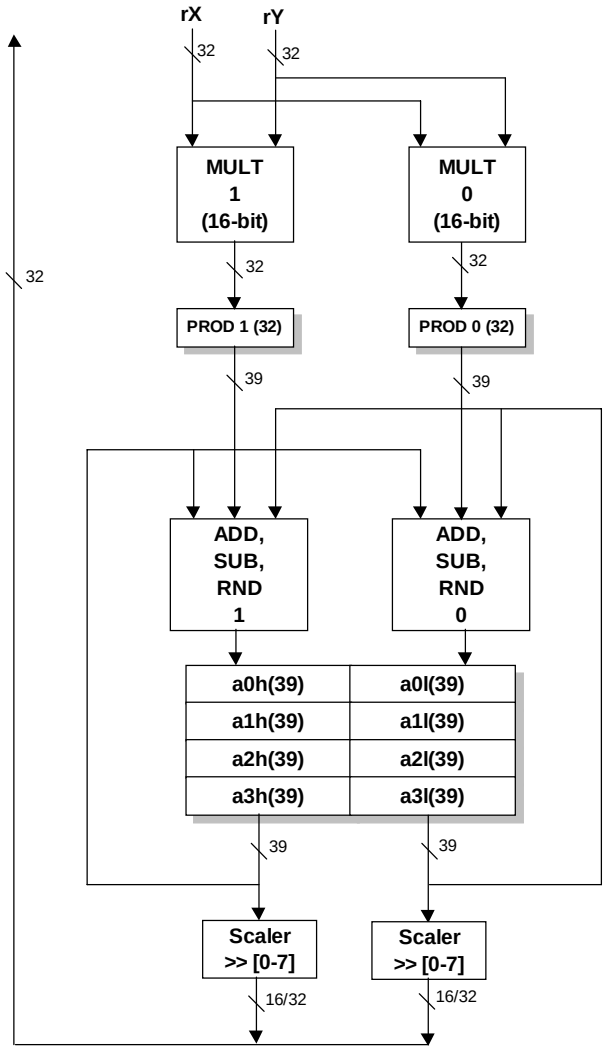
Architecture: SIMD Multiply-Accumulate

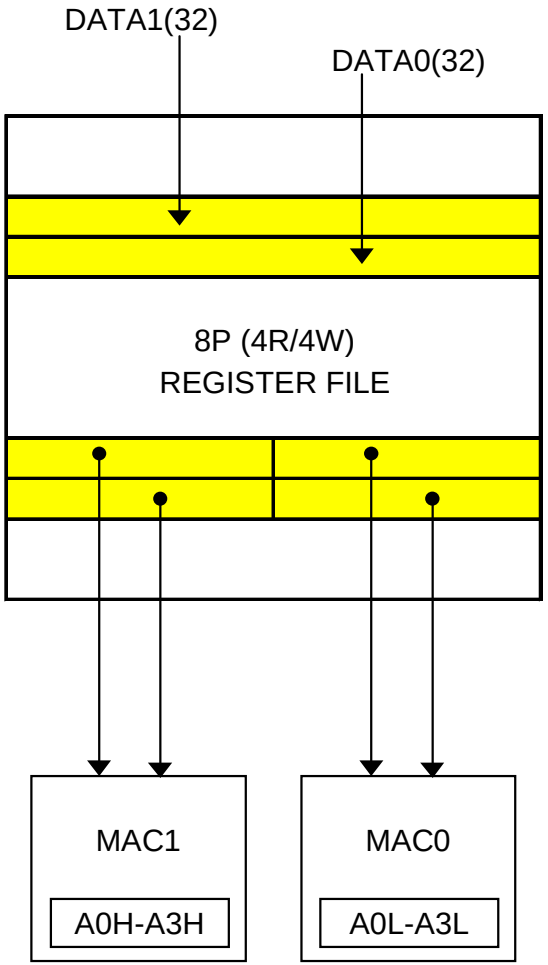
- Dual 16-bit/32-bit MACs
- Pipelined for single-cycle 16-bit multiply-accumulate
- High-fidelity DSP arithmetic
  - optional saturate
  - fractional arithmetic mode
  - guard bits
  - rounding
  - support for bit-exact telecom standards



Architecture: Bandwidth/Execution Balance

- "Twinword" Load/Stores of 32-bit general-register pairs sustain two (2) MACs/cycle

Pipe B	Pipe A
…	LT reg, MEM
…	LT reg, MEM
…	LT reg, MEM
MADD aM, rX, rY	LT reg, MEM
MADD aM, rX, rY	…
MADD aM, rX, rY	…
MADD aM, rX, rY	…



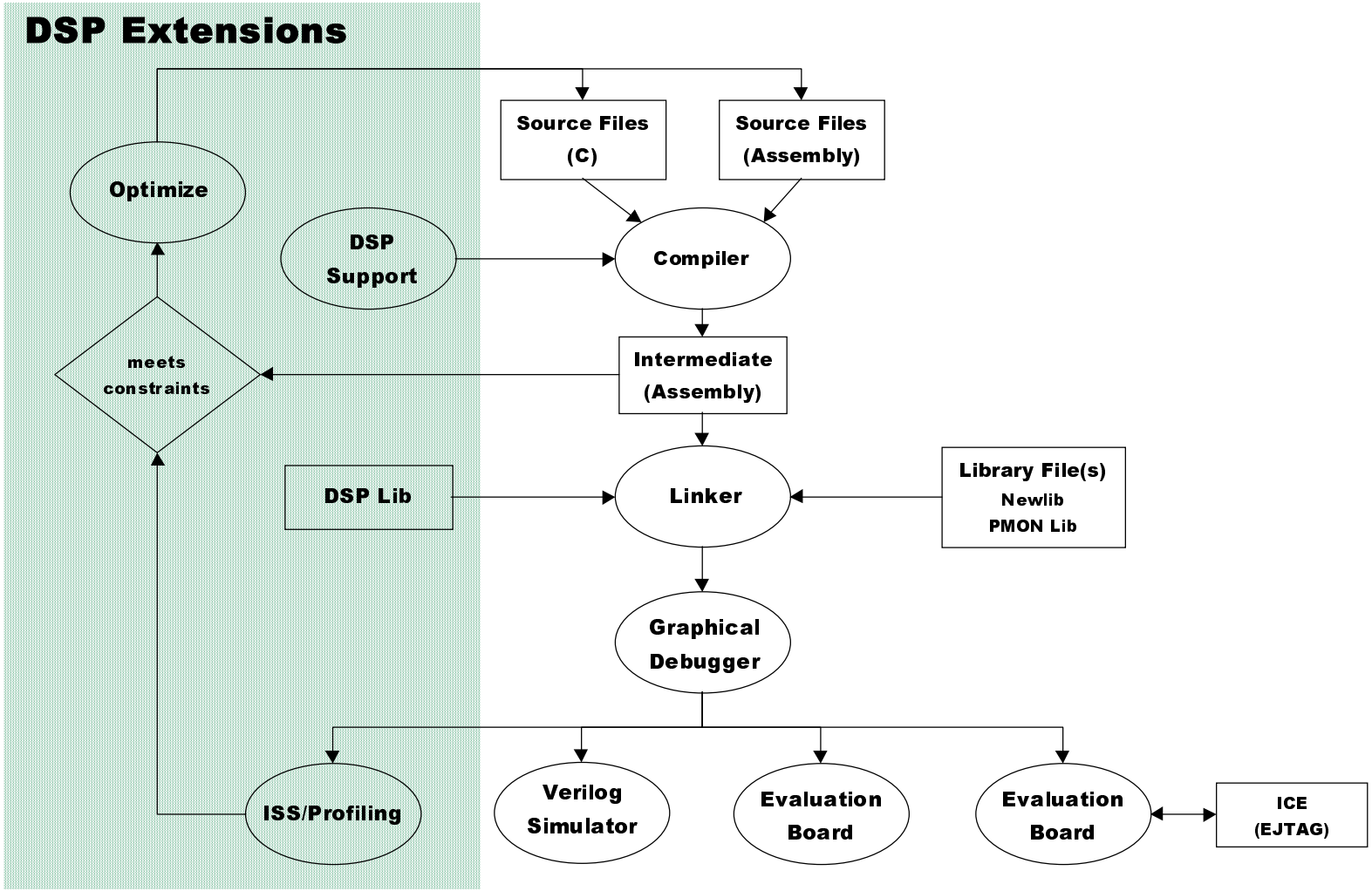
Instruction Set: DSP Extensions to MIPS®

NEW INSTRUCTION		DESCRIPTION
macop2[.s]	aM, rX, rY	· single or dual 16-bit (mult, madd, msub) · single-cycle throughput · optional saturate
multop	aM, rX, rY	· 32-bit integer multiply · [16-bit, 16-bit] complex multiply
accop[.s] rnda2 mta2 mfa2	aD, aS, aT aM[, n] rX, aM rX, aM[, n]	· accumulator ops (add, sub) · optional saturate (.s) · optional alignment shift (n)

Instruction Set: DSP Extensions (cont.)

NEW INSTRUCTION	DESCRIPTION
aluop2[.s] rD, rS, rT	· dual 16-bit versions of all MIPS I ALU ops · six new DSP ALU ops · optional saturate (.s)
loadop [.cN] rT, (pnt)stride storeop [.cN] rT, (pnt)stride	· postmodified pointers · optional circular buffers (.cN)
cmv[cond] rD, rS, rT	· conditional moves
blcnzl rT, destination	· branch on loop count not zero, auto decrement

Program Development: RISC-DSP Tool Flow



Implementation: Licensing Model

- RTL (Available: Nov 99)
  - Verilog source code
  - Configuration tool (lconfig)
  - Synthesis and timing scripts
  - Testability scripts
  - Regression suite
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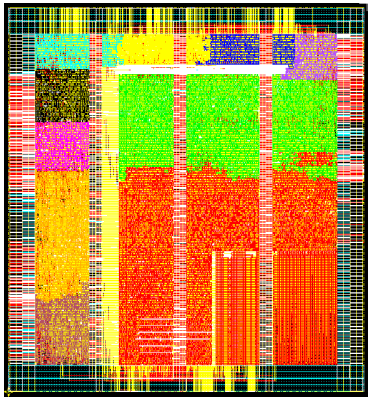
  -
- SmoothCore™ (Available: Feb 00)
  - GDS2 database
  - Verilog simulation models
  - Synthesis and timing models
  - 99.5% fault coverage vectors
  - Regression suite

```
wire        PI_STMODE_N = STMODE_N;
wire        PI_SIN      = SIN;

assign CCRhold          = PO_CCRhold;
assign CChold           = PO_CChold;

always @(posedge CLK) begin
  if (!RESET_D2_R_N) begin
      CFG_CEENBL_D1_R   <= CFG_CEENBL;
    end
  end
```



Implementation: Technology

	POWER OPTIMIZED	PERFORMANCE OPTIMIZED
Technology	0.18μm CMOS 4-layer metal	0.18μm CMOS 4-layer metal
Circuit Design	Single-edge, fully-static, standard cell	Single-edge, fully-static, standard cell
Voltage	1.0 Volts	1.8 Volts
System Clock	50 MHz	200 MHz
Peak Performance	100 MMACs	400 MMACs
Area (excludes RAMs)	5.5 mm^2	6 mm^2
Power (worst case)	20 mW	225 mW
MMACs/mm^2	18	67
mW/MHz	0.4	1.1

Implementation: Benchmarks

Algorithm	Cycles	Example (200 MHz)
Dot Product (2 vectors, length N)	0.625 N + 8	0.84 μsec (N = 256)
Real FIR (N coefficients, M samples)	(0.5N + 4) M	10 μsec (N = 32, M = 100)
Complex FIR (N coefficients, M samples)	(2N + 4) M	34 μsec (N = 32, M = 100)
Complex FFT (N-point, radix-2)	$\log_2$ N (3.25N + 10) + 2.25N + 40	179 μsec (N = 1024)

Summary

The **LX5280** has extended the scope of the MIPS architecture and tool chain into a wide range of DSP applications.