The Ultra Data UD3000
A Next Generation Video Processor Core

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Outline

- The challenge of high-definition video
- Architectural approaches
- Block diagrams
- Architecture for optimal performance
- Data flow
- Application: HD video decoder chip

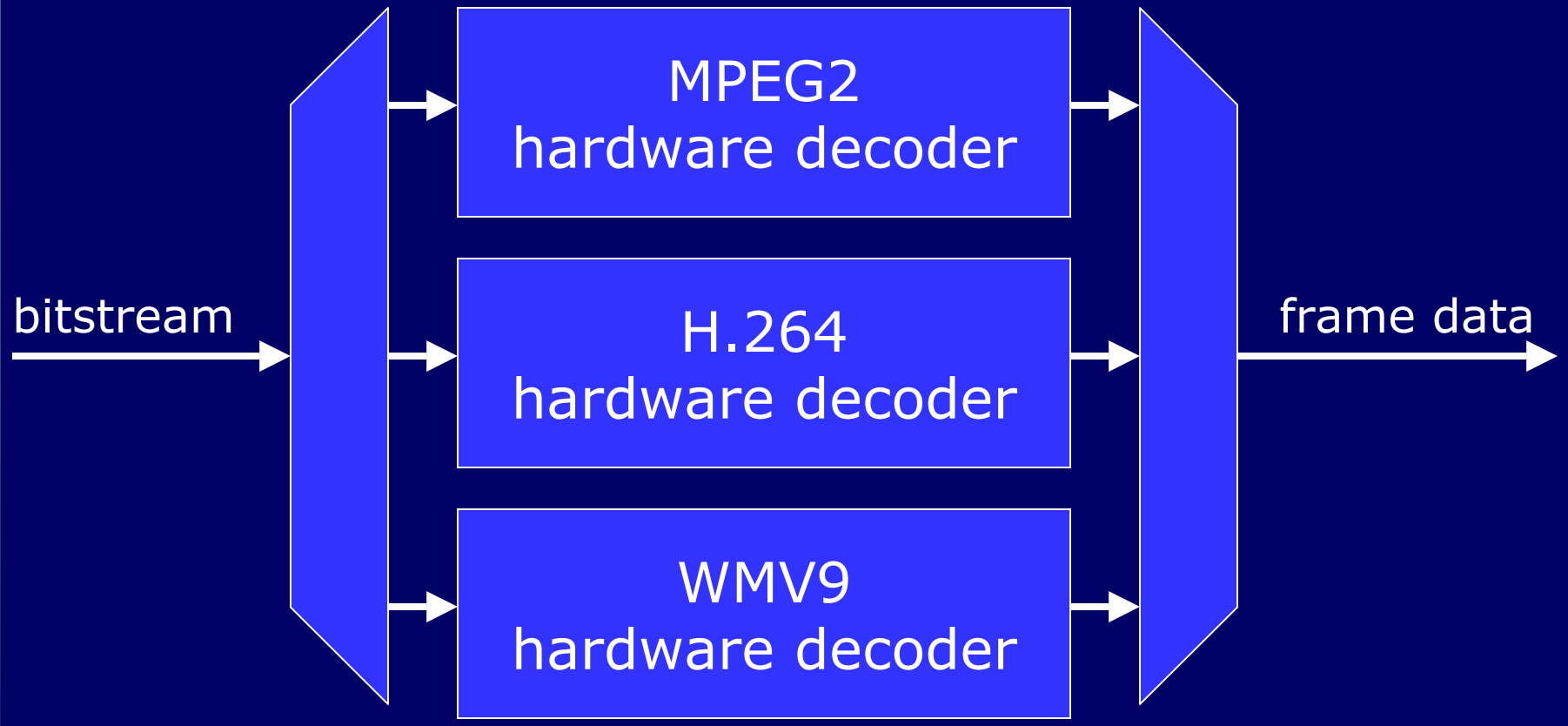
High Definition

- HDTV consumer products are coming
  - DVD players
  - Digital cable receivers
  - Digital satellite broadcast receivers
  - Personal video recorders
- HDTV has 6x the pixels of SDTV
  - 63 megapixels per second
- Next generation compression algorithms are needed to meet bandwidth and storage constraints

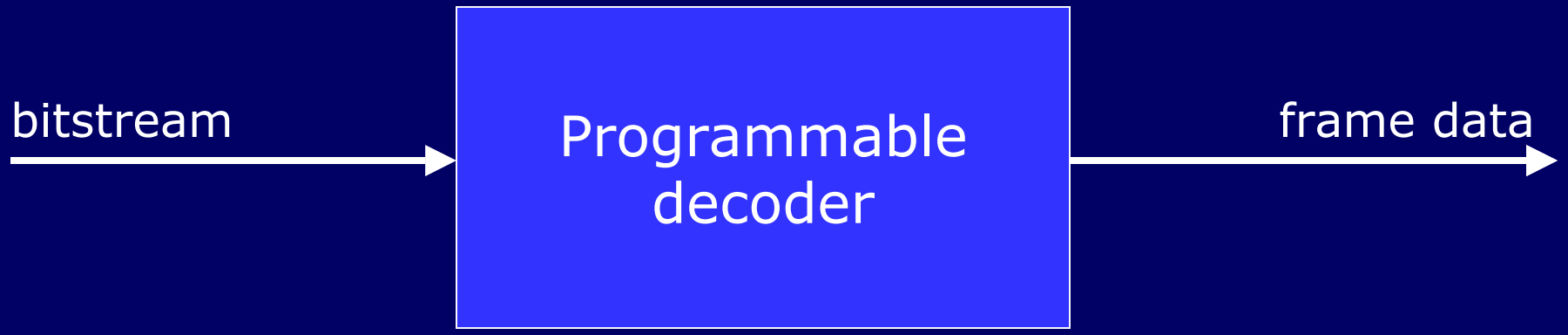
Next Generation Codecs

- Many next generation codecs:
  - ITU-T/ISO H.264 MPEG4 Part 10 AVC
  - Microsoft Windows Media Video 9
  - On2 Technologies VP6
- ~10x as many decisions in outer loop code
  - —CABAC bitstream compression
  - —Nine intra prediction modes
  - —Variable pixel block sizes, down to 4x4
  - —Motion vector dependent deblocking filter
- RISC architectures do not have sufficient performance
- High performance DSPs are too costly

Hardwired Approach



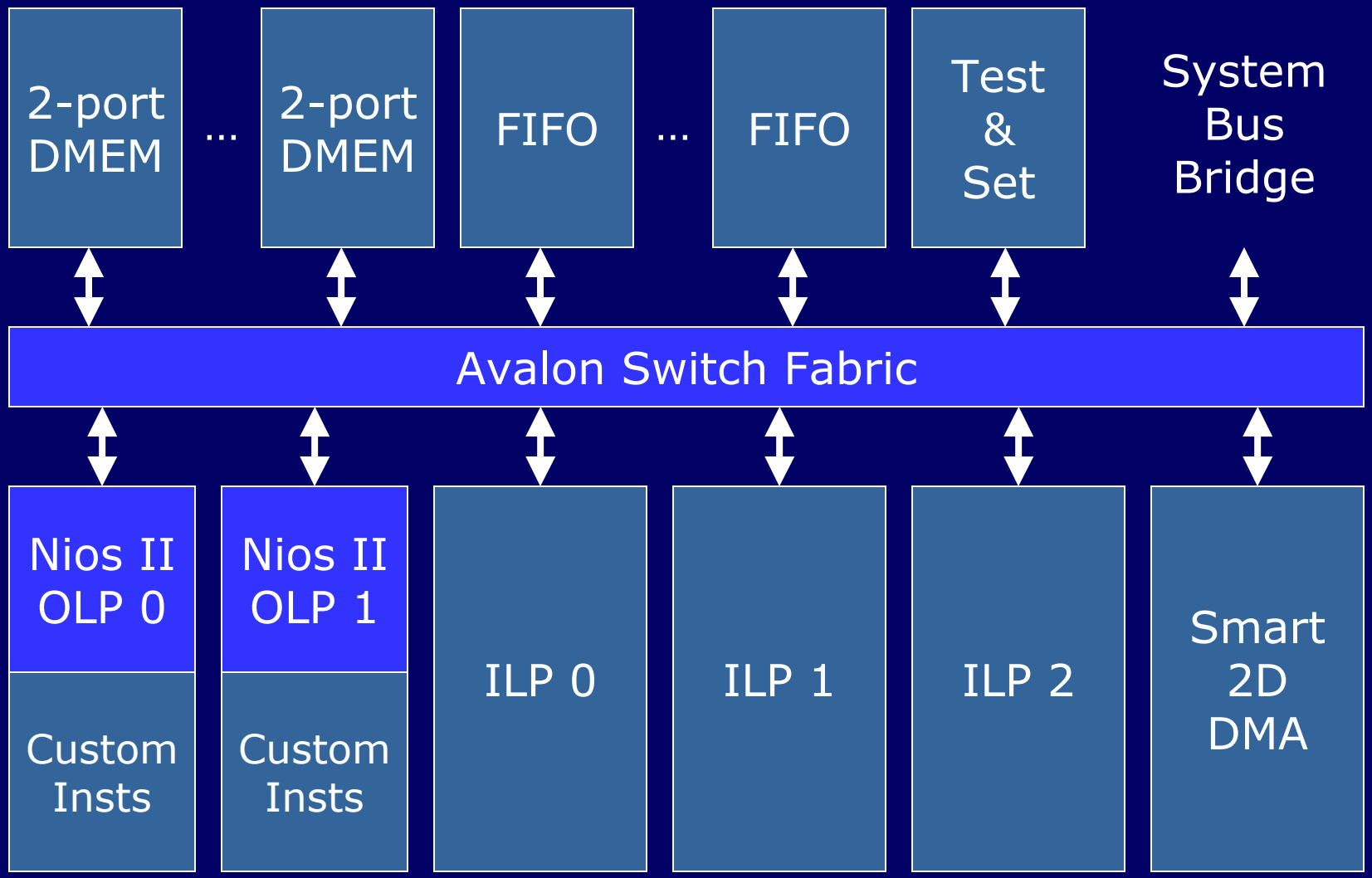
Programmable Approach



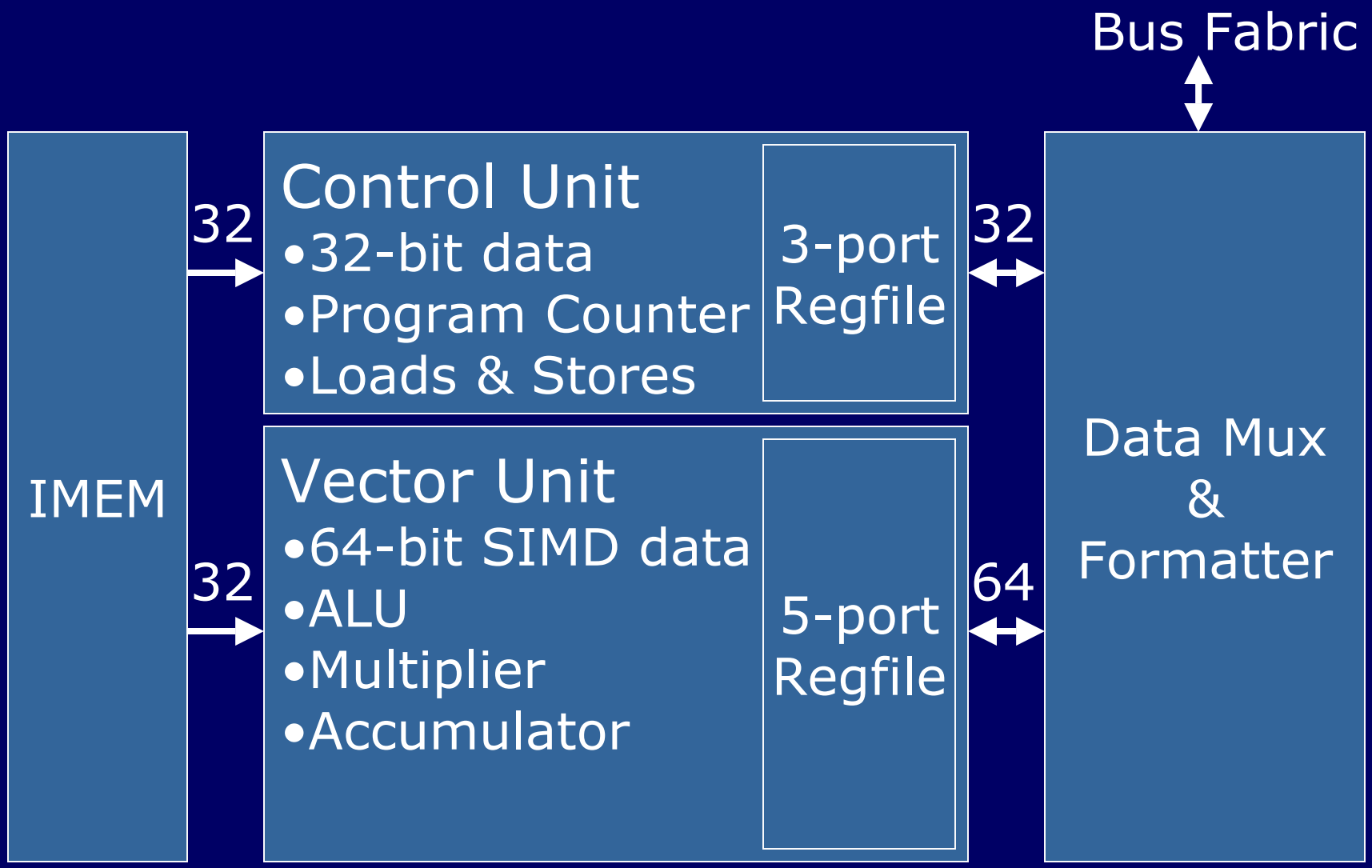
UD3000 Key Features

- Multiprocessor architecture for pipelined dataflow
- Outer loop processors (OLPs) for high level decision making
- Inner loop processors (ILPs) for pixel processing
  - 32-bit control unit (CU)
  - 64-bit vector unit (VU)
- Shared 64-bit dual-port DMEMs & FIFOs for moving data between processors
- Smart 2D DMA controller for main memory access without stalls

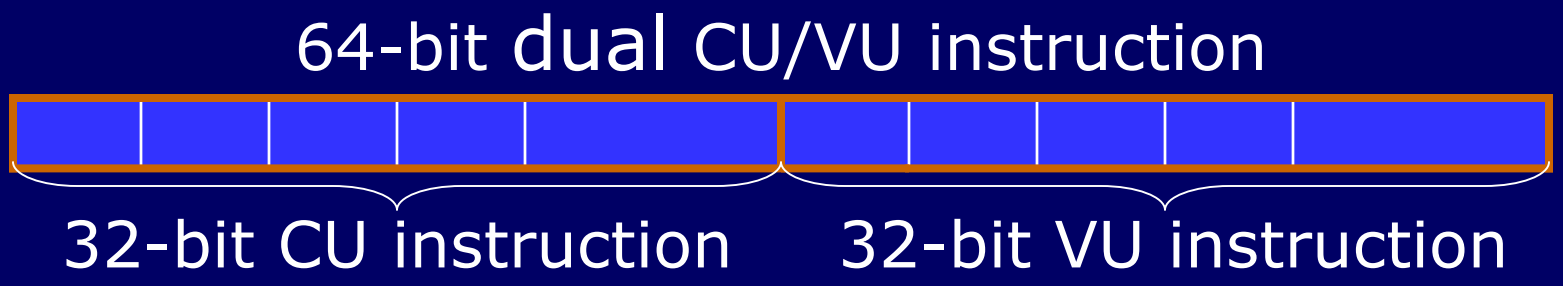
UD3000 Block Diagram



ILP Diagram


Bus Fabric
IMEM
32
32
Control Unit
•32-bit data
•Program Counter
•Loads & Stores
3-port Regfile
Vector Unit
•64-bit SIMD data
•ALU
•Multiplier
•Accumulator
5-port Regfile
32
64
Data Mux & Formatter

ILP Programming



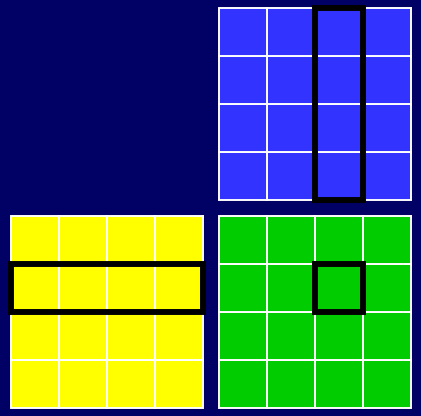
- CU & VU operate in lock-step
- CU manages address calculation and data load/store
- VU performs SIMD data processing

```
// CU INSTRUCTION     // VU INSTRUCTION
vlwbx  v6, 0(r3)    ; mult    Acc0, v1, v2
vlwbx  v7, 4(r3)    ; madd    Acc0, v1, v3
mfv    r10, v21     ; madd    Acc0, v1, v4
addi   r10, r10, 4  ; madd    Acc0, v1, v5
mtv    v21, r10     ; mult    Acc1, v1, v6
slt    r4, r1, r9   ; madd    Acc1, v1, v7
mfa    v3, Acc0     ; and     v11, v0, v0
bnez   r4, loop     ; pack    v4, v3, 3
vsw    v4, 0(r2)    ; mergel8 v10, v4, v4
addi   r1, r1, 16   ; sle8    v0, v10, v20
```

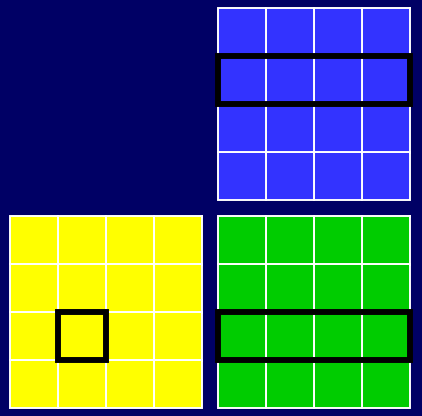
Multiplier Throughput

- 12 fixed-point 16-bit MACs per cycle
  - No sources of processor stalls
  - CU moves data to keep VU fed
- Round, shift, saturate data transforms performed during move from accumulator
- Move from accumulator can be performed by CU

Broadcast Multiply



Transpose,
SIMD multiply,
reduction add



SIMD
broadcast
multiply

- Eliminates transpose
- Eliminates intermediate storage
- Eliminates reduction add

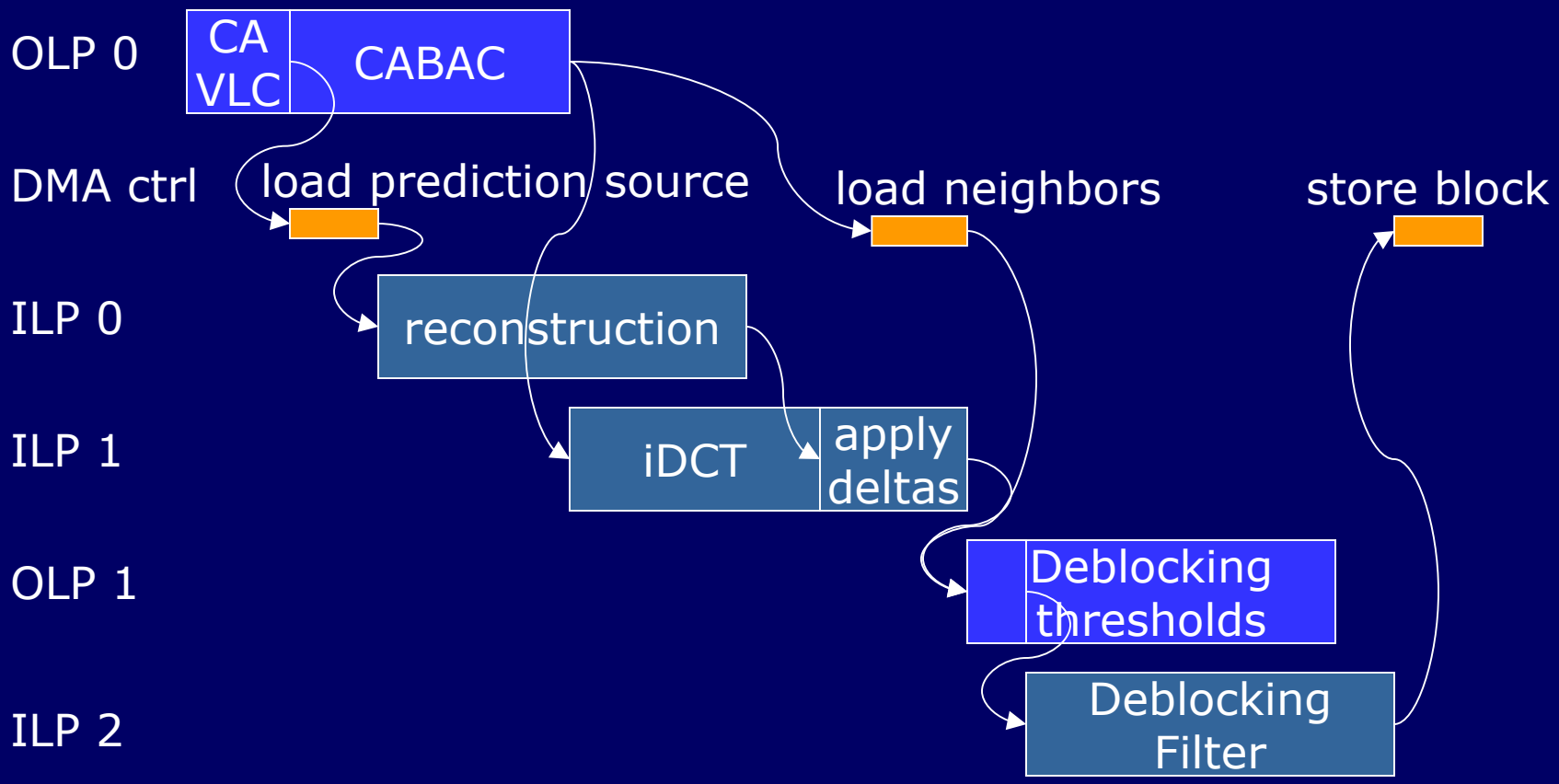
ILP Speed Enhancements

- No MMU or FPU
  - No TLB lookup paths
- 2 branch delay slots
  - No branch prediction required
- 2 load delay slots
  - Full cycle for data memory access
  - Full cycle for data mux and formatter
- No cache
  - No tag compare

DMA Controller

- Processors with caches spend significant time stalled for the service of misses
- Video data access patterns are regular
- A 2D DMA controller yields better performance than caches
  - Smaller: no cache control/prediction logic
  - Faster & deterministic: no stalls
  - The cost: software overhead

Per Block Decode



UD3000 Statistics

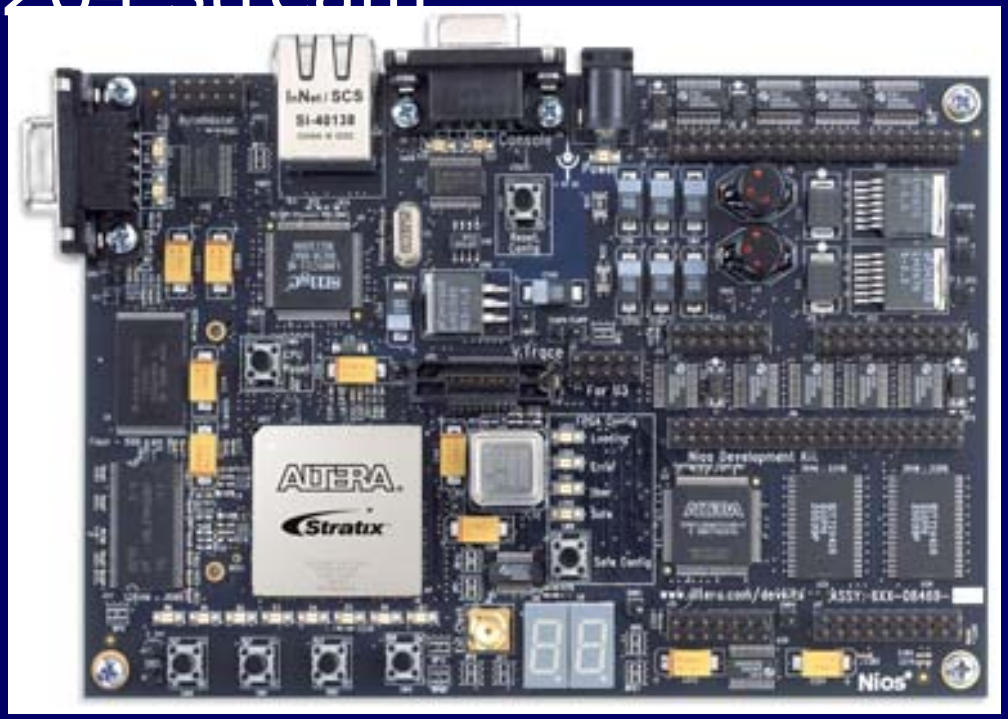
Deliverable	Synthesizable soft core and software for industry-leading codecs
Architecture	Shared memory multiprocessor
Technology	130 nm target (portable)
Speed	400 MHz worst case
Throughput	4.8 GMACS
Performance	H.264 Main Profile Level 4.1

FPGA Video Decode

- Demo available from Altera and Ultra Data
- Decode of an H.264 stream
- Ultra Data RTL and software
- H.264 Main Profile at SDTV resolution at

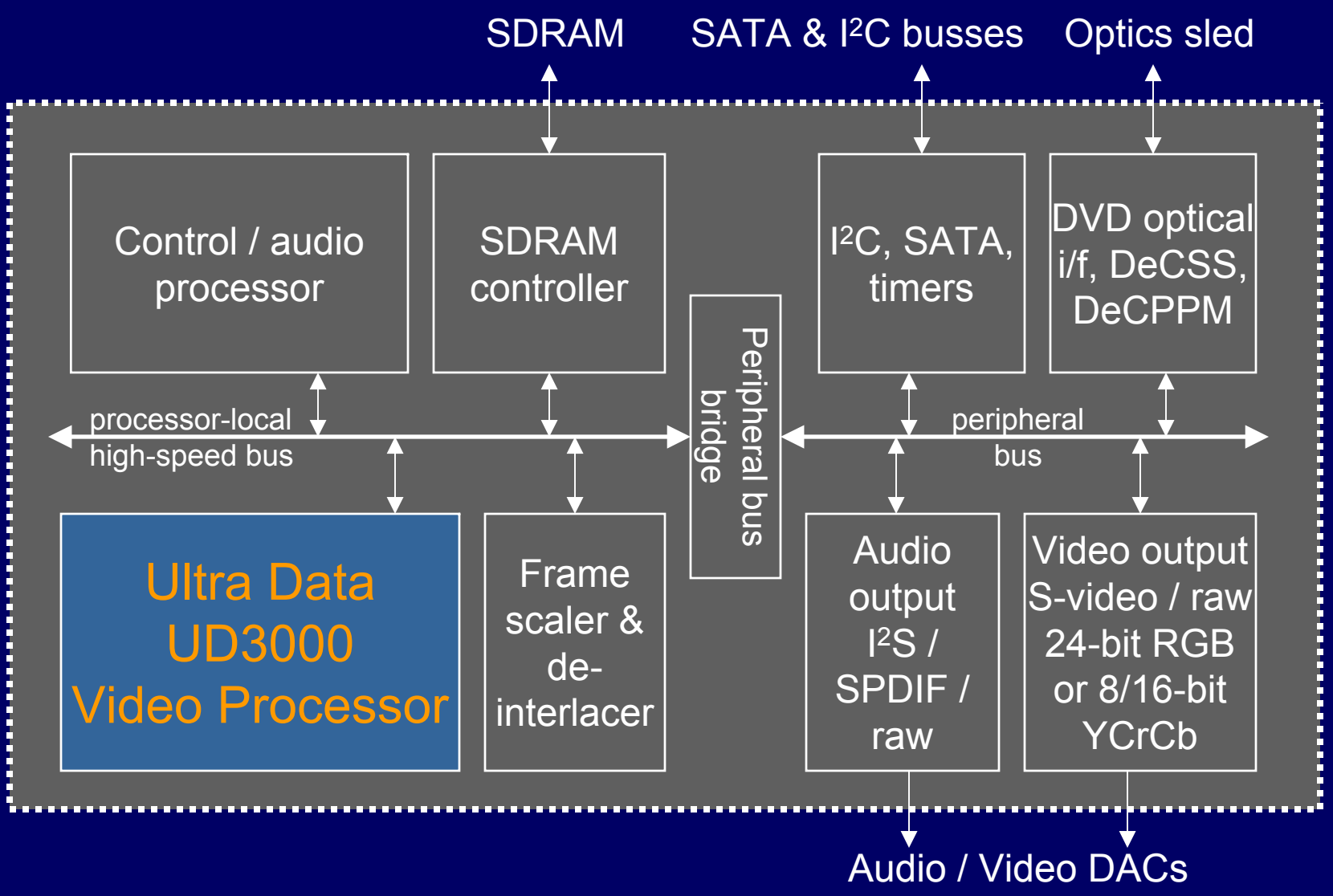
  75 MHz
- HDTV achievable in silicon at

  400 MHz



Altera Nios Development Kit
Stratix Professional Edition

Video Decoder Chip



Summary

- Next generation consumer video requires six to ten times the processing power
- The UD3000 provides this through its video optimized architecture
  - Shared memory multiprocessor for a pipelined data flow
  - An inner loop processor with a speed optimized architecture and 4.8 GMACS for matrix multiplication
  - A smart DMA memory interface